REMARKS:

Minor changes are made to this specification. Claims 4 and 7 are amended; marked up versions of the amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). Specifically, claims 4 and 7 have been written in independent format to place the claims in proper U.S. format. New claims 16-18 are added. Claims 1-18 are pending in the application. Reexamination and reconsideration of the application, as amended, are respectfully requested.

Art-based Rejections

Claims 1 and 4

Claims 1-7 were rejected under 35 U.S.C. 103(a) as being unpatentable over Bird et al. (USPN 5,852,425) further in view of Strobel et al. (USPN 5,420,600).

Applicant respectfully submits that the cited references fail to teach or suggest that "each of the master IC and the at least one slave IC has an input terminal for receiving the display control signal output from the display control signal generation section of the master IC through an external wiring," as required by claims 1 and 4.1/ The Examiner concedes that Bird et al. fail to teach of suggest "a master IC and at least one slave IC." The Examiner cites Strobel et al. as teaching these missing recitations. However, as shown in FIG. 5 of the Strobel et al. reference, Applicant submits that neither the master nor the slave has an input terminal for receiving the display control signal output from the display control signal generation section of the master IC through an external wiring." The signal input SIN shown in FIG. 5 is not a "**display control signal output from** the display control signal generation section of **the master IC through an external wiring**," as required by claims 1 and 4. Rather, as discussed at col. 13, lines 1-4 of

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1/ Exemplary benefits associated with some embodiments of the present invention are discussed, for example, at p. 3, lines 26 - p. 4, lines 14 and p. 19, line 16 – p. 20, line 19 of the present application.

Strobel, "SIN is the data input via which data bits can be transferred serially from the microprocessor in synchronism with the clock pulses SCK." As discussed at col. 7, lines 50-60 of Strobel, "short codes supplied by the microprocessor are supplied in each case to the signal input SIN of the shift register of the first IC IC1." (Emphasis added.)

Thus, Applicant respectfully submits that the cited references fail to teach or suggest at least the above recitations of claim 1. Accordingly, Applicant respectfully submits that claim 1 is patentable over the cited references. In addition, Applicant respectfully submits that dependent claims 2 and 3 are patentable at least by virtue of their dependency from independent claim 1. Applicant further submits that independent claim 4 is patentable for at least the same reasons, and that dependent claims 16 and 17 are patentable at least by virtue of their dependency from independent claim 4.

Claims 5 and 7

Claims 1-7 were rejected under 35 U.S.C. 103(a) as being unpatentable over Bird et al. (USPN 5,852,425) further in view of Strobel et al. (USPN 5,420,600).

Applicant respectfully submits that the cited references fail to teach or suggest a master IC comprising "an internal delay circuit which delays the display control signal." The Examiner concedes that Bird et al. fail to teach of suggest "a master IC and at least one slave IC." The Examiner cites Strobel et al. as teaching these missing recitations. However, as shown in FIG. 5 of the Strobel et al. reference, there is nothing in Strobel et al. that indicates that the master includes an internal delay circuit "which delays the display control signal," as required by claims 5 and 7.

Applicant further respectfully submits, for at least the reasons described above with respect to claims 1 and 4, that the cited references fail to teach or

suggest that "the at least one slave IC has an input terminal for receiving the display control signal output from the output terminal of the master IC through an external wiring," as required by claims 5 and 7.

Thus, Applicant respectfully submits that the cited references fail to teach or suggest at least the above recitations of claim 5. Accordingly, Applicant respectfully submits that claim 5 is patentable over the cited references. In addition, Applicant respectfully submits that dependent claim 6 is patentable at least by virtue of its dependency from independent claim 5. Applicant further submits that independent claim 7 is patentable for at least the same reasons, and that new dependent claim 18 is patentable at least by virtue of its dependency from independent claim 7.

Claim 8

Claims 8-9 and 12-13 were rejected under 35 U.S.C. 102(a) as being anticipated by S-MOS System, Inc., Dot Matrix liquid crystal display Driver SED 1520/21 Version 1.0 (October, 1996) (hereinafter "SMOS").

Applicant respectfully submits that the cited SMOS reference fails to teach or suggest that "the display control signal generation section is enabled and the display control signal is output from the output terminal when the display driver IC is set as a master by the selection terminal" or "wherein the display control signal generation section is disabled when the display driver IC is set as a slave by the selection terminal," as required by claim 8. Rather, the 2.1 SYSTEM BLOCK DIAGRAM shown at page 7 of the SMOS reference, simply shows that when VDD is input to M/S terminal of SED 1520, then the master driver will be selected, whereas when VSS is input to M/S terminal of SED 1520, then the slave driver will be selected. M/S selection changes the function of pins FR, COM0-COM15, OSC1 (CS) and OSC2 (CL). The common scanning order for the slave driver is the reverse of the master driver. Figure 7.3 at page 41 shows that a resistor Rf can be placed

between OSC1 of the master and OCS2 of the slave. However, there is nothing in the SMOS reference that would suggest that "the **display control signal generation section is enabled** and the **display control signal is output** from the output terminal when the display driver IC is set as a master by the selection terminal" or "wherein the **display control signal generation section is disabled** when the display driver IC is set as a slave by the selection terminal," as required by claim 8. The SMOS reference simply fails to discuss enabling or disabling of a "**display control signal generation section**."

Thus, Applicant respectfully submits that the cited references fail to teach or suggest at least the above recitations of claim 8. Accordingly, Applicant respectfully submits that claim 8 is patentable over the cited references. In addition, Applicant respectfully submits that dependent claims 9-11 are patentable at least by virtue of their dependency from independent claim 8.

Claim 12

Claims 8-9 and 12-13 were rejected under 35 U.S.C. 103(a) as being unpatentable over S-MOS System, Inc., Dot Matrix liquid crystal display Driver SED 1520/21 Version 1.0 (October, 1996) (hereinafter "SMOS").

For at least the reasons discussed above with respect to claim 8, Applicant respectfully submits that the cited references fail to teach or suggest "wherein the **display control signal generation section is enabled**, and the **display control signal** generated in the display control signal generation section **is output through the output terminal and input to the internal delay circuit**, when the display driver IC is set as a master by the selection terminal," or that "the **display control signal generation section is disabled** when the display driver IC is set as a slave by the selection terminal," as required by claim 12.

In addition, Applicant respectfully submits that the cited SMOS reference fails to teach or suggest "an **internal delay circuit** which delays the display control signal generated in the display control signal-generating circuit," as required by claim 12. Applicant further respectfully submits that the cited references fail to teach or suggest "a **signal selection circuit for selecting** the transition state of the logic of one of the display control signal **input through the internal delay circuit** and the display control signal **input through the input terminal**," as required by claim 12. The cited SMOS reference fails to teach or suggest these claim recitations.

Thus, Applicant respectfully submits that the cited references fail to teach or suggest at least the above recitations of claim 12. Accordingly, Applicant respectfully submits that claim 12 is patentable over the cited references. In addition, Applicant respectfully submits that dependent claims 13-15 are patentable at least by virtue of their dependency from independent claim 12.

The art made of record but not relied upon by the Examiner has been considered. However, it is submitted that this art neither describes nor suggests the presently claimed invention.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: December 10, 2002

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Version with markings to show changes made:

4. (Amended) An electronic apparatus [comprising the electro-optical device as defined in claim 1] including an electro-optical device comprising:

a display section which includes a plurality of first electrodes extending in a first direction, a plurality of second electrodes extending in a second direction crossing the first direction, and electro-optical elements driven by the first and second electrodes;

a first driver which drives the first electrodes; and

a second driver which drives the second electrodes,

wherein the first driver has a master IC for driving a first group of the first electrodes, and at least one slave IC for driving a second group of the first electrodes;

wherein the master IC has a display control signal generation section which generates a display control signal based on a signal from an external MPU; and wherein each of the master IC and the at least one slave IC has an input terminal for receiving the display control signal output from the display control signal generation section of the master IC through an external wiring.

7. (Amended) An electronic apparatus [comprising the electro-optical device as defined in claim 5] including an electro-optical device comprising:

a display section which includes a plurality of first electrodes extending in a first direction, a plurality of second electrodes extending in a second direction crossing the first direction, and electro-optical elements driven by the first and second electrodes;

a first driver which drives the first electrodes; and

a second driver which drives the second electrodes,

wherein the first driver has a master IC for driving a first group of the first electrodes and at least one slave IC for driving a second group of the first electrodes;

wherein the master IC comprises:

a display control signal generation section which generates a display control signal based on a signal from an external MPU;

an internal delay circuit which delays the display control signal; and

an output terminal which outputs the display control signal before the display control signal passes through the internal delay circuit; and

wherein the at least one slave IC has an input terminal for receiving the display control signal output from the output terminal of the master IC through an external wiring.